PRESS RELEASE

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Coupling Wave Solutions (CWS) provides Power Estimation for the ATHOLE Project on Low Power and Microprocessor Systems.

Coupling Wave Solutions S.A. is providing applications software from its WaveIntegrity™ Noise Coupling Analysis platform to the ATHOLE Project on Low Power and Microprocessor Systems. This significant project has 5 major contributors: STMicroelectronics, providing architecture and low-power design methodologies, Thales, who contribute the application, CEA-LETI, who provide the IPs and low power methodology, Verimag, contributing the scheduling and tools, and CWS, who are delivering power estimation.

ATHOLE, initiated in 2007 as a Minalogic collaborative research project, is focused on the delivery of both methodology and IPs providing low power design for complex, multi processor SoCs. In particular, this group is supporting the P2012 Architecture template, with its synchronous computing, redundant grain, SMP clusters, with voltage and frequency islands.

Methodologies and supporting applications capable of providing clear and practical techniques in the development of such a complex SoC fabric will find use in the majority of SoC design environments of the next 3-5 years. As of today, there exists a strong barrier that separates architecture-level and system-level design from the physical world. This can be

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seen in the usage of mathematical and/or empirical expressions used to optimize power consumption in the early design stages. As power consumption is becoming a major challenge in 45nm and below, this gap is anticipated to lead to undesired and lengthy correction loops.

Power consumption is one of the aspects requiring simultaneous verification (that the eventual silicon will consume at most what is allowed by the standard) and optimization (to get the best performance/consumption compromise). What is available now, in existing flows, provides physical estimations very late in the flow.

The primary goal of ATHOLE is to provide physical power consumption models, algorithms and IPs earlier in the design flow, to help both verification and optimization.

“Through our contribution to the ATHOLE project, CWS and our partners want to enable our joint customers to analyse designs’ complex power requirements and avoid the, frequently related, noise coupling issues that beset large ICs/SoCs, while reducing the need for overly conservative design practices.”, commented Brieuc Turluche, CEO of Coupling Wave Solutions. “These capabilities are critical in quickly identifying power and noise coupling-related problems seen in silicon, and not just with SNA, but including the other critical components of interconnect and package/pcb analysis. They are essential in helping locate and answer potential issues, both before tape- out and even earlier in the design process, from the floorplanning stage.”

“In LETI’s provision of complex IPs and algorithms, access to more physical-based models helps us fill the gap between the software and physical implementations”, says, Laurent Malier, CEO of CEA-LETI. “The collaboration between CWS and CEA-LETI has

brought particular benefits related to the capture of power consumption for any combination of digital, analog and/or RF blocks."

"For those implementing complex designs commercially, the ability to include power-consumption optimization while handling the scheduling of algorithms on a multi-core architecture is key," said Bruno JEGO of STMicroelectronics and ATHOLE project leader. "This ability is extremely valuable when available from early in the design process, as intended by ATHOLE, rather than late in the process when changes are almost impossible."

About Coupling Wave Solutions.

Coupling Wave Solutions (CWS) has developed a solution for avoiding noise-related problems in integrated circuit (IC) design. Its WaveIntegrity™ platform dramatically reduces the impact of noise when combining analog or RF and digital blocks in a single die or in a system in package (SiP), and is helping designers avoid both the traditional issues (for example, spurs and jitter) that coupling noise brings, while also allowing them to quickly prepare solid noise avoidance strategies for the newer nodes of 22nm and below.

For more information, visit the Coupling Wave Solutions website www.cwseda.com, email to info@cwseda.com. Or call:

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