Users Reduce Risk in Three Main Areas, Providing Verification Previously Impossible

March 06, 2013 -- Coupling Wave Solutions S.A. (CWS), a leader in solutions for noise analysis in complex A/MS SoC designs, announced that **STMicroelectronics** has adopted the WaveIntegrity™ analysis tools to remove risk caused by on-chip, package and PCB parasitics. Following multiple evaluations, covering use for both CMOS and FD-SOI processes, a leading contender for next-generation low-power products fabrication, STMicroelectronics is deploying WaveIntegrity™ across groups designing complex IP, Digital Convergence Products and Automotive devices.

CWS has worked closely with STMicroelectronics to ensure its teams have full visibility of potential noise issues in their IP and SoC designs. As a result, STMicroelectronics users of WaveIntegrity benefit from a proven, flexible and highly differentiated verification solution.

"Minimizing power while maximizing performance and securing functionality is driving STMicroelectronics's adoption of new tools and methodologies. The comprehensive CWS noise analysis solution has enabled our teams to successfully identify and avoid significant noise issues in mixed-signal SOCs," said Philippe Magarshack, STMicroelectronics Executive Vice President. "The close and ongoing cooperation with CWS is helping our teams achieve success with next-generation designs incorporating advanced analog and digital IPs, across a range of processes, including our latest advances in FD-SOI."

STMicroelectronics has used WaveIntegrity™ to analyze 28nm FD-SOI SOCs, minimize power-supply bumps and pin count, analyze digital noise on I/Os in 55nm CMOS automotive designs, and ensure mixed digital and RF ICs are clean of noise issues, at 40nm and below. This has required the development of methodologies appropriate to the specific requirements of each type of design, as well as the wider adoption of more "standard" techniques enabled by WaveIntegrity™.

"The complexity and frequency of SoC designs increase year-on-year, together with increasingly stringent power requirements. Successfully verifying the noise characteristics of the SoCs, the package they are placed in and the PCBs they are inserted on, has become an increasingly difficult challenge: applying "rules of thumb" is no longer adequate. The capabilities of WaveIntegrity™ provide and support such analysis, and enable verification previously considered impractical by other means," commented Brieuc Turluche, president and CEO of CWS. "With multiple teams contributing to each design it is essential that noise analysis is both easy and rapid to implement at each stage."

To learn more visit www.cwseda.com.

Source: Coupling Wave Solutions S.A.

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Comment by Francois Clement, CTO, Coupling Wave Solutions:

Our work with ST, over the past 3 years, has been both a challenge and a pleasure.

The sophisticated functionality of ST's SoCs demands that cutting edge IP be assembled into ever more complex and power-efficient designs. However well this IP is designed, how it behaves when placed in situ depends on many factors. That said, it must work.

Our joint results are demonstrating that WaveIntegrity™ helps teams at both the IP developmental stage and when the SoC is being brought together.

For both the IP developers and those doing good-inwards testing on third party IP, WaveIntegrity™ aids in the design and evolution of IP to ensure it is as robust against noise-related issues as possible. Previously, undertaking such analysis, especially when the team may be spread over two or three continents, as not been feasible. By breaking the tasks into well defines, and frequently automated, activities, we have brought capabilities to bear that any IP design team can employ.

This has also required us to develop new methodologies, both to address the needs of such complex development in the newer processes and nodes, but also to align with ST's own methodologies. The twin challenge, of still keeping a baseline methodology from which others can adapt to meet their own flows, is a pretty interesting, if usual, one..

For SoC integration teams, we found that the sooner they can start modelling the impact of noise on the various analog IP they are receiving, the better. This meant allowing the initial analysis to run on the design with a considerable number of IPs represented by (our automatically generated) approximations of what would eventually be used. As the various blocks are delivered so the analysis is refined with the real noise signatures. Teams have found potential issues very much earlier than they would have. Indeed, many have previously waited for silicon to come back before even attempting to investigate potential noise issues.

In working with teams assembling large (> 50M gates) SoCs, we have also found we can address issues by virtue of our dual frequency and time domain approaches, which have frequently been tried using other tools and methods and which have failed. That said, there is still room for intelligent preparation before trying to analyse the biggest devices.

The other fascinating dimension we work with is keeping up with the development and introduction of the new process nodes. While most of our history has involved standard CMOS processes, from 180nm- 40nm, for several years we have been addressing the needs of both FD-SOI and FinFet. Both have their particular characteristics with respect to noise propagation, and working closely with the development teams allows us to tune what we can provide. Our work is all about risk reduction, and

that is particularly important when teams, and their companies, are venturing onto lower (and more complex nodes) or completely new processes.

For such people, the level of complexity they have to deal with would seem to be increasing in every direction. The more we can do to reduce the risks this complexity brings, particularly in noise analysis, enables them to focus on other problem areas. We have also found that knowing the *actual* parameters for noise, rather than the usual rules of thumb developed over years, allows considerable advantages in, for example, decision on the required power and ground pins required for the various IP. Teams can make well educated choices rather than follow “rules of thumb”, which are often very conservative and over protective, or guidance from the IP developers who usually state rather over-protective requirements for their IP in use!

We see the application of WaveIntegrity™ increasing rapidly, as the mixed signal nature and complexity of SoCs continued to increase. It provides relief for not just the design team, to know there will be no noise coupling issues before they sign-off, rather than having to wait for the silicon to return! Helping ensure such designs come back “noise clean” is the real pleasure.

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